IN THE CLAIMS

Please amend the claims as follows.

Claims 1-20 (Cancelled).

21. (Previously Presented) A multiplier circuit, comprising:

a partial products generator capable of receiving a multiplicand value and a multiplier value and generating a plurality of partial products;

a first summing array capable of summing a first subset of the partial products to produce a first summation value; and

a second summing array capable of summing a second subset of the partial products to produce a second summation value;

wherein at least one of:

at least some of the partial products in the first subset are non-sequential ones of the plurality of partial products; and

at least some of the partial products in the second subset are non-sequential ones of the plurality of partial products.

22. (Previously Presented) The multiplier circuit of Claim 21, wherein:

the first subset comprises even ones of the plurality of partial products; and

the second subset comprises odd ones of the plurality of partial products.

23. (Previously Presented) The multiplier circuit of Claim 21, wherein:

the first summing array comprises a first plurality of adders; and

the second summing array comprises a second plurality of adders.

24. (Previously Presented) The multiplier circuit of Claim 23, wherein each of the first plurality of adders and the second plurality of adders comprises a carry-save adder.

25. (Previously Presented) The multiplier circuit of Claim 21, further comprising an adder capable of summing the first summation value and the second summation value to produce a third summation value.

26. (Previously Presented) The multiplier circuit of Claim 25, wherein:

the first summation value comprises a first N-bit sum value and a first N-bit carry value;

the second summation value comprises a second N-bit sum value and a second N-bit carry value; and

the third summation value comprises a third N-bit sum value and a third N-bit carry value.

27. (Previously Presented) The multiplier circuit of Claim 26, further comprising a second adder capable of adding the third N-bit sum value and the third N-bit carry value to produce a 2N-bit resulting sum value and a 1-bit resulting carry value.

28. (Previously Presented) The multiplier circuit of Claim 27, wherein:

the adder comprises a carry-save adder; and

the second adder comprises a carry-propagate adder.

29. (Previously Presented) A data processor, comprising:

a plurality of pipelined execution units, at least one of the pipelined execution units comprising a multiplier circuit;

the multiplier circuit comprising:

a partial products generator capable of receiving a multiplicand value and a multiplier value and generating a plurality of partial products;

a first summing array capable of summing a first subset of the partial products to produce a first summation value; and

a second summing array capable of summing a second subset of the partial products to produce a second summation value;

wherein at least one of:

at least some of the partial products in the first subset are non-sequential ones of the plurality of partial products; and

at least some of the partial products in the second subset are non-sequential ones of the plurality of partial products.

30. (Previously Presented) The data processor of Claim 29, wherein:

the first subset comprises even ones of the plurality of partial products; and

the second subset comprises odd ones of the plurality of partial products.

31. (Previously Presented) The data processor of Claim 29, wherein:

the first summing array comprises a first plurality of adders; and

the second summing array comprises a second plurality of adders.

32. (Previously Presented) The data processor of Claim 31, wherein each of the first plurality of adders and the second plurality of adders comprises a carry-save adder.

33. (Previously Presented) The data processor of Claim 29, wherein the multiplier circuit further comprises:

a first adder capable of summing the first summation value and the second summation value to produce a third summation value, wherein the first summation value comprises a first N-bit sum value and a first N-bit carry value, the second summation value comprises a second N-bit sum value and a second N-bit carry value, and the third summation value comprises a third N-bit sum value and a third N-bit carry value; and

a second adder capable of adding the third N-bit sum value and the third N-bit carry value to produce a 2N-bit resulting sum value and a 1-bit resulting carry value.

34. (Previously Presented) The data processor of Claim 33, wherein:

the first adder comprises a carry-save adder; and

the second adder comprises a carry-propagate adder.

35. (Previously Presented) The data processor of Claim 29, wherein:

the multiplier circuit comprises one of a plurality of multiplier circuits; and

the plurality of multiplier circuits comprises a first multiplier in a floating point unit and a second multiplier in an integer unit.

36. (Currently Amended) A method, comprising:

generating a plurality of partial products using a multiplicand value and a multiplier value at a partial products generator;

summing a first subset of the partial products to produce a first summation value; and

summing a second subset of the partial products to produce a second summation value;

wherein at least one of:

at least some of the partial products in the first subset are non-sequential ones of the plurality of partial products; and

at least some of the partial products in the second subset are non-sequential ones of the plurality of partial products.

37. (Previously Presented) The method of Claim 36, wherein:

the first subset comprises even ones of the plurality of partial products; and

the second subset comprises odd ones of the plurality of partial products.

38. (Previously Presented) The method of Claim 36, wherein:

summing the first subset of the partial products comprises summing the first subset of the partial products using a first plurality of adders; and

summing the second subset of the partial products comprises summing the second subset of the partial products using a second plurality of adders.

39. (Previously Presented) The method of Claim 38, further comprising:

summing the first summation value and the second summation value to produce a third summation value using a third adder, wherein the first summation value comprises a first N-bit sum value and a first N-bit carry value, the second summation value comprises a second N-bit sum value and a second N-bit carry value, and the third summation value comprises a third N-bit sum value and a third N-bit carry value; and

summing the third N-bit sum value and the third N-bit carry value to produce a 2N-bit resulting sum value and a 1-bit resulting carry value using a fourth adder.

40. (Previously Presented) The method of Claim 39, wherein:

each of the first plurality of adders and the second plurality of adders comprises a carry-save adder;

the third adder comprises a carry-save adder; and

the fourth adder comprises a carry-propagate adder.

41. (New) A processor, comprising:

at least one pipelined execution unit comprising a multiplier, the multiplier capable of:

generating a plurality of partial products using a multiplicand value and a multiplier value;

summing a first subset of the partial products to produce a first summation value; and

summing a second subset of the partial products to produce a second summation value;

wherein at least one of:

at least some of the partial products in the first subset are non-sequential ones of the plurality of partial products; and

at least some of the partial products in the second subset are non-sequential ones of the plurality of partial products.